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Pin FMEA for AUP family

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Document information

Info	Content
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Abstract	This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of the NXP Semiconductors' AUP family under typical failure situations

Revision history

Rev	Date	Description
v.1	20110506	initial version

Contact information

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1. Introduction

The NXP ultra-low-power (AUP) CMOS logic 74AUP1G/2G3Gxxx family is designed for high-performance, low-power applications. These low-voltage, Si-gate CMOS devices offer the industry's lowest dynamic power consumption in a logic device.

2. AUP family overview

The NXP 74AUP1G/2G/3Gxxx family of Si-gate CMOS devices uses advanced process technology and next-generation packaging technology to create extremely small devices that consume very little power. The devices are available in single- (1Gxx), dual- (2Gxx) and triple-gate (3Gxx) formats.

AUP devices offer the industry's lowest power dissipation capacitance (C_{PD}), yet maintain low propagation delays (t_{PD}) and superior ESD protection. Typical C_{PD} at 1.8 V and 3.3 V is only 4.3 pF, while the t_{PD} at a V_{CC} of 2.5 V is only 2.5 ns.

Operating over a very wide supply range of 0.8 V to 3.6 V, AUP devices are ideally suited for use in mixed-voltage applications. Schmitt-trigger action at all inputs improves noise immunity by making the circuit tolerant to slower input rise and fall times across the entire range of supply voltage.

The devices extend battery life by ensuring very low power consumption that is 30 % lower than competing logic functions. To save even more battery power, the devices are fully specified for partial power-down applications that use the I_{OFF} feature. The I_{OFF} circuitry disables the output, preventing damage caused by backflow current passing through the device when it is powered down.

AUP devices are available in PicoGate and MicroPak packages, which are roughly ten times smaller than a conventional SO14 package. PicoGate and MicroPak products reduce time-to-market by making it easy to implement last-minute changes. They also improve the cost-effectiveness of crowded layouts by simplifying routing and eliminating dependencies in intricate line-layout patterns.

The AUP family operates over an extended temperature range (–40 °C to +125 °C) that is suitable for a wide range of applications, including portable, consumer, automotive, and military. Multi-pin (5-, 6- and 8-pin) packages make it easy to select the right combination of features.

3. Pin FMEA

This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of the NXP Semiconductors' AUP family under typical failure situations such as a short-circuit to V_{CC} or GND or to a neighboring pin, or if a pin is left open.

Some AUP family devices have special functions, such as translators and level-shifters, that can have different behaviors.

A failure is classified according to its effect on the AUP device and the functionality of the application; see Table 1.

Table 1. Classification of failure effects

Class	Failure effect
A	damage to device
	affects application functionality
B	no damage to device
	may affect application functionality
C	no damage to device
	no affect to application functionality

Table 2. FMEA matrix for pin short-circuit to V_{CC}

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality
Output	C	if output defined HIGH, no damage, no leakage, no output level change
Output	A	if output defined LOW, short-circuits and high currents can damage device, output level changes
GND	B	short-circuits and high currents can damage device, will affect functionality

Table 3. FMEA matrix for pin short-circuit to GND

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality
Output	C	if output defined LOW, no damage, no leakage, no output level change
Output	A	if output defined HIGH, short-circuits and high currents can damage device, output level changes
V_{CC}	B	no damage to device, will affect functionality

Table 4. FMEA matrix for pin left open

Pin	Class	Remarks
Input	B	undefined operating condition, no damage, increases leakage, may affect functionality
Output	C	normal operating condition, no damage, no leakage
GND	B	undefined operating condition, no damage, increases leakage, will affect functionality
V_{CC}	B	undefined operating condition, no damage, increases leakage (only for I/O types), will affect functionality

Table 5. FMEA matrix for pin short-circuits between neighbor pins

Pin	Class	Remarks
Input to input	C	if inputs have same voltage levels: no damage, no leakage
	B	if inputs have different voltage levels: leakage increases, will affect functionality

Table 5. FMEA matrix for pin short-circuits between neighbor pins *...continued*

Pin	Class	Remarks
Input to output	A	if input and output have different voltage levels, can cause high current and can damage device, will affect functionality
	C	if input and output have same voltage levels, no damage, no leakage
Input to GND	-	see Table 3
Input to V_{CC}	-	see Table 2
Output to output	C	if outputs have same voltage levels, no damage, no leakage
	A	if outputs have different voltage levels, can cause high current and can damage device, will affect functionality
Output to input	-	same effect as 'input to output' condition
Output to GND	-	see Table 3
Output to V_{CC}	-	see Table 2
GND to V_{CC}	-	not applicable, these pins are not neighbors

4. Abbreviations

Table 6. Abbreviations

Acronym	Description
AUP	Advanced Ultra-low Power
CMOS	Complementary Metal-Oxide Semiconductor
EDP	Electronic Data Processing
ESD	ElectroStatic Discharge
FMEA	Failure Modes and Effects Analysis
LVC	Low-Voltage CMOS
TTL	Transistor-Transistor Logic

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